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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,226	09/02/2003	Ammar Derraa	3882.8US (99-0017.08/US)	4741

24247 7590 11/24/2004

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EXAMINER	
SANTIAGO, MARICELI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,226	DERRAA, AMMAR	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-18* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Amendment, filed on September 15, 2004, has been entered and acknowledged by the Examiner.

Claims September 15, 2004 are pending in the instant application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3, 7, 8 and 10-16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,017,772. Although the conflicting claims are not identical, they are not patentably distinct from each other for the following reasons.

U.S. Application SN 10/654,226	U.S. Patent No. 6,017,772
Claim 1 claims a method for fabricating at least one emission structure, comprising forming at least one conductive structure extending across at least a portion of a substrate, substantially removing a longitudinal portion of the at least one conductive structure to define at least one conductive layer having a width that is	Claim 18 states a method for fabricating at least one emission structure, comprising disposing a layer of conductive material over a substrate of the field emission array, patterning the layer to define a plurality of substantially mutually parallel conductive lines and removing at least a substantially longitudinal center

oriented substantially perpendicular to the substrate, the substrate being exposed along a length of the at least one conductive layer, and forming at least one emission structure adjacent the at least one conductive layer	portion of the selected ones of the plurality of conductive lines (a width that is oriented substantially perpendicular to the substrate being inherently present since disposing a layer conveys a layer having a thickness, length and width), the substrate exposed between the plurality of conductive lines (thus, along a length) the emitter tips formed by patterning a semiconducting layer disposed over and between the parallel conductive lines.
Claim 2 claims a method wherein forming the at least one emission structure includes forming an emitter tip.	Claim 18 states a method forming emitter tips by patterning a semiconducting layer disposed over and between the parallel conductive lines.
Claim 3 claims a method wherein forming the at least one emission structure further includes forming a resistor corresponding to the at least one emitter tip.	Claim 18 states a method which defines emitter tips and their corresponding resistors.
Claim 4 claims a method wherein forming the resistor comprises forming the resistor adjacent to the at least one conductive layer.	Claim 18 state a method which simultaneously forms emitter tips and their corresponding resistors between parallel conductive lines, thus both elements are considered to be adjacent to at least one conductive layer.
Claim 7 claims a method wherein forming the at least one conductive structure comprises, disposing a layer comprising conductive material over the substrate, and patterning the layer.	Claim 18 states a method comprising disposing a layer of conductive material over a substrate, patterning the layer to define a plurality of substantially mutually parallel conductive lines.
Claim 8 claims a method wherein forming the at least one emission structure comprises forming the at least one emission structure from at least one of semiconductive material and conductive material.	Claim 18 states a method comprising disposing another layer comprising semiconductive material or conductive material and patterning the another layer to substantially simultaneously define the emitter tips and their corresponding resistors
Claim 10 claims a method for fabricating at least one emission structure, comprising forming at least one conductive structure that extends at least partially across a	Claim 18 states a method for fabricating at least one emission structure, comprising disposing a layer of conductive material over a substrate of the field emission array,

substrate, forming at least one emitter tip and a corresponding resistor adjacent to the at least one conductive structure, and substantially removing at least a longitudinal portion of the at least one conductive structure along substantially an entire length thereof to define at least one conductive layer having a width that is oriented substantially perpendicular to the substrate.	disposing a layer comprising semiconductive material or conductive material and patterning the layer to substantially simultaneously define the emitter tips and their corresponding resistors, patterning the conductive layer to define a plurality of substantially mutually parallel conductive lines and removing at least a substantially longitudinal center portion of the selected ones of the plurality of conductive lines (a width that is oriented substantially perpendicular to the substrate being inherently present since disposing a layer conveys a layer having a thickness, length and width).
Claim 11 claims a method wherein forming the at least one conductive structure comprises disposing a layer comprising conductive material on the substrate and patterning the layer.	Claim 18 states a method comprising disposing a layer of conductive material over a substrate of the field emission array, patterning the layer to define a plurality of substantially mutually parallel conductive lines
Claim 12 claims a method wherein forming the at least one emitter tip comprises forming the at least one emitter tip from at least one of semiconductive material and conductive material.	Claim 18 states a method comprising forming emitter tips by patterning a semiconducting layer disposed over and between the parallel conductive lines.
Claim 13 claims a method wherein forming the corresponding resistor comprises forming the corresponding resistor from at least one of semiconductive material and conductive material.	Claim 18 states a method comprising disposing a layer comprising semiconductive material or conductive material over the plurality of conductive lines, and patterning the layer to substantially simultaneously define the emitter tips and their corresponding resistors.
Claim 14 claims a method wherein forming the at least one emitter tip comprises: disposing at least one layer comprising at least one of semiconductive material and conductive material over the substrate and the at least one conductive structure, removing a longitudinal portion of at least one region of the at least one layer located over the at	Claim 18 states a method comprising: disposing a layer comprising semiconductive material or conductive material over the plurality of conductive lines and regions of the substrate exposed between the plurality of conductive lines, patterning the layer to expose a substantially longitudinal center portion of each of the selected ones of the plurality of conductive lines, and

least one conductive structure to expose at least a substantially longitudinal portion of the at least one conductive structure, and patterning at least one remaining portion of the at least one layer.	removing at least a substantially longitudinal center portion of the selected ones of the plurality of conductive lines.
Claim 15 claims a method wherein patterning the at least one remaining portion of the at least one layer includes defining the at least one emitter tip from the at least one layer.	Claim 18 states a method comprising: disposing a layer comprising semiconductive material or conductive material over the plurality of conductive lines and regions of the substrate exposed between the plurality of conductive lines patterning the layer to substantially simultaneously define the emitter tips.
Claim 16 claims a method wherein patterning the at least one remaining portion of the at least one layer further includes forming the corresponding resistor.	Claim 18 states a method comprising: disposing a layer comprising semiconductive material or conductive material over the plurality of conductive lines and regions of the substrate exposed between the plurality of conductive lines patterning the layer to substantially simultaneously define the emitter tips and their corresponding resistors.

Claims 5, 9, 17 and 18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,017,772 in view of U.S. Patent 6,276,982 to Derraa.

U.S. Application SN 10/654,226	U.S. Patent No. 6,017,772 in view of U.S. Patent No. 6,276,982
Claim 5 claims a method wherein forming the at least one emission structure comprises forming a plurality of lines of emission structures. Claims 9 and 18 claim a method wherein forming the at least one emission structure comprises forming at least one emission structure so as to extend over a lateral edge of the at least one	Claim 11 of Patent '982 states a method comprising the steps of forming lines of emitter tips and corresponding resistors over portions of the substrate exposed between adjacent conductive structures, each of the lines extending over a lateral edge of at least one of the distinct conductive structures adjacent thereto.

conductive structure.	It would have been obvious to one having ordinary skill in the art to provide emitter structures comprising a plurality of lines of emission structures extending over a lateral edge of at least one of the distinct conductive structures, since such modification would have been recognized as an obvious matter of design engineering.
Claim 17 claims a method wherein substantially removing comprises leaving at least a lateral edge of the at least one conductive structure along substantially its entire length thereof.	Claim 11 of Patent '982 states a method comprising the steps of substantially removing at least longitudinal portions of the distinct conductive structures to expose the substrate between adjacent lines without removing the lateral edge. It would have been obvious to one having ordinary skill in the art to provide a lateral edge of the at least one conductive structure along substantially its entire length thereof, since such modification would have been recognized as an obvious matter of design engineering.

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 6, the references of the Prior Art of record fails to teach or suggest the combination of the limitations as set forth in claim 6, and specifically comprising the limitation of electrically isolating at least one emission structure located along a first line of the plurality of lines from at least one emission structure located along an adjacent, second line of the plurality of lines.

Response to Arguments

Applicant's arguments with respect to claims 1-5 and 7-18 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11/19/04
Mariceli Santiago
Patent Examiner
Art Unit 2879